164-GHz MMIC HEMT Doubler

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***Abstract*—In this letter, a MMIC frequency doubler based on InP HEMT and grounded CPW (GCPW) technology is reported. The doubler demonstrated a conversion loss of only 2 dB and output power of 5 dBm at 164 GHz. The 3-dB output power bandwidth is 14 GHz, or 8.5%. This is the best reported result for a MMIC HEMT doubler above 100 GHz.**

***Index Terms*—MMIC frequency converters, MODFETs.**

I. Introduction

RECENTLY, there has been a considerable interest in utilizing frequencies above 100 GHz for a variety of applications, including radiometry and atmospheric sensors. One of the ways for generating sources at these frequencies is by frequency multiplication. HEMT-based frequency multipliers have several advantages over diode-based multipliers. HEMT multipliers typically consume less dc power, dissipate less heat, and have better conversion gain/loss. Additionally, HEMT multipliers can be monolithically integrated with oscillators and amplifiers. For example, a 94-GHz single chip source was demonstrated using InP HEMT-HBT technology [1].

Several HEMT doublers have been reported [1]–[3], including a balanced 40-GHz HEMT doubler with 1-dB conversion loss at an input power of 5 dBm [2]. The highest frequency HEMT doubler is a 180-GHz MMIC with a 6-dB conversion loss at an input power of 0 dBm [3]. For comparison, a 94-GHz Schottky diode doubler demonstrated 6-dB conversion loss at 55 mW of output power [4].

In this letter, we report a 164-GHz doubler with only 2-dB conversion loss at 7 dBm of input power. This translates into 5 dBm or 3.2 mW of output power. This design utilizes HRL Laboratories' AlInAs/GaInAs/InP HEMT with maximum oscillation frequency (f_{max}) of 600 GHz. The transmission lines are realized using grounded coplanar waveguide (GCPW) technology. The GCPW design was chosen for its advantages over microstrip in terms of improved gain characteristics obtained by eliminating source via holes and related parasitics.

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II. Device Modeling

The doubler is designed using a 0.1-μm T-gate AlInAs/GaInAs/InP HEMT device with 4×37 μm gate periphery. The device exhibits a dc transconductance of 1050 mS/mm, breakdown voltage of 4 V, and extrinsic cut-off frequency (f_τ) of at least 180 GHz.

The design of an active doubler requires nonlinear analysis; therefore, a large signal HEMT model was first developed. The Curtice quadratic model was chosen due to its simplicity. More complicated models such as Curtice cubic or Angelov [2] might be more accurate, but require intensive measurement and modeling. Additionally, Curtice quadratic model is readily available in commercial simulators, like Agilent's Series IV or ADS. The device S-parameters were measured on a wafer from 1–110 GHz using a TRL calibration. From these measurements, the parasitic elements and intrinsic capacitances were determined.

III. Doubler Design

First step in designing a doubler is choosing a bias point. Like a power amplifier, doublers can be biased to operate in a class A or B regime [3], [5]. A class B doubler is biased at pinch-off and channel conducts in pulses having a duty cycle near 50%. Class A doublers are biased near the peak transconductance (g_m) point. Class B doublers are typically more stable, efficient, and provide higher output power, while class A doublers can have higher conversion gain.

A class B doubler is designed using a harmonic balance simulator from Agilent's Series IV. The matching elements are realized using GCPW lines. Airbridges are used at each discontinuity to suppress undesired slot mode excitation. HEMT device, with f_{max} of 600 GHz, has a high gain at frequencies below 60 GHz. In order to suppress possible oscillations at these frequencies, a low pass filter was designed. It consists of coupled GCPW lines and it also serves as a dc block. The filter was designed using Bay Technology's IE3D full-wave moment method software. Large decoupling capacitors and 20-Ω or 100 -Ω epi-resistors are added in the drain or gate bias line, respectively, to suppress biasing oscillations. The fundamental frequency at the output is suppressed using a quarter-wave open stub, which presents short at the fundamental and open at the second harmonic.

Fig. 1 shows a photograph of the fabricated MMIC doubler. The chip size is 1.1×1.2 mm^2. The doubler was fabricated on a 3" wafer, which was then thinned to 50 μm. The process also includes a wet-etched backside via holes for parallel plate mode suppression. The substrate was thinned in order to make fabrication of via holes easier. The high density of vias is necessary

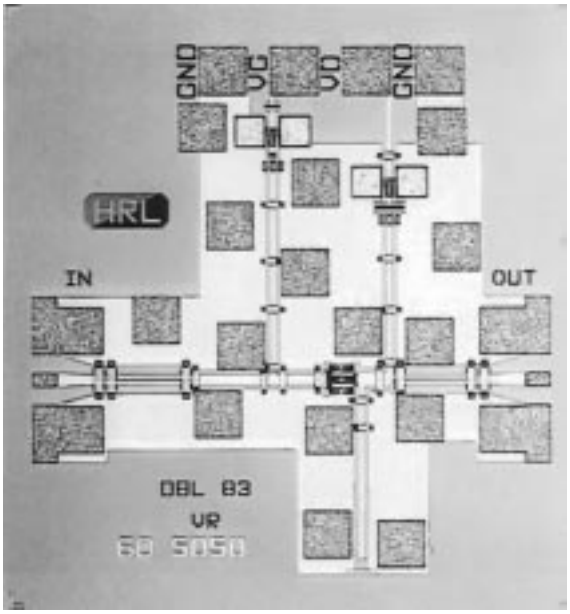

Fig. 1. Photograph of the fabricated MMIC doubler. The die size is 1.32 mm^2.

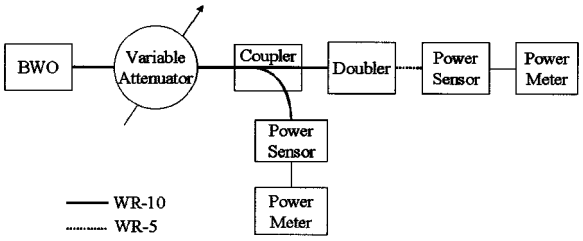

Fig. 2. Test setup used for measuring doubler's performance.

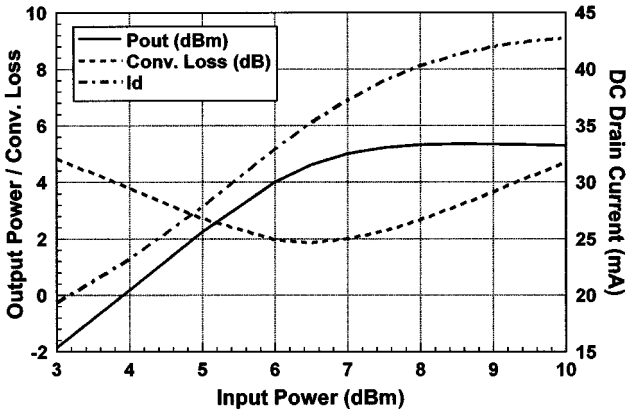

Fig. 3. Measured doubler's conversion loss, output power, and DC drain current versus input power at the output frequency of 164 GHz.

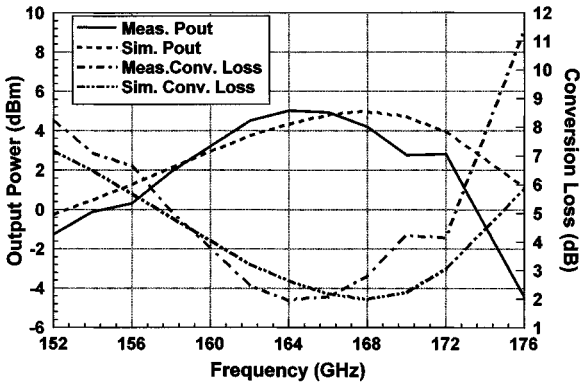

Fig. 4. Measured and simulated doubler's conversion loss and output power versus frequency. Input power is set to 7 dBm.

to suppress the undesired parallel plate mode, which can propagate energy into the substrate.

IV. Measured and Simulated Results

Fig. 2 shows the setup used for doubler power measurement. The 70 to 110 GHz signal is generated by a Resonance Instrument's back wave oscillator (BWO). The RF drive level is adjusted using a Millitech WR-10 Precision attenuator. The input power is measured using a 10 dB coupler and a HP power sensor and power meter. The measurements were done on a wafer. The chip input is provided with a GGB Industries' WR-10 RF probe and the chip output is connected to the GGB Industries' WR-5 RF probe. The output is then connected to the Anritsu's WR-5 power sensor and power meter.

This setup was then used to measure doubler's output power versus input power and frequency. The best results were obtained at the input frequency of 82 GHz. Fig. 3 shows the output power, conversion loss, and dc drain current versus input power at 82 GHz. The measurement was done for a drain bias supply of 2.54 V and gate bias supply of -0.6 V, which corresponds to the pinch-off condition. A conversion loss of 2 dB is measured at an input power of 7 dBm. This corresponds to an output power of 5 dBm or 3.2 mW at 164 GHz. The RF efficiency, defined as $P_{\rm out}(2\omega)/P_{\rm in}(\omega)\times 100\%$, of this doubler is 63%. To our knowledge, this is the best conversion loss and output power result for HEMT doublers above 100 GHz.

Fig. 3 also shows the dc drain current which increases with increased input power. This self-biasing effect is the same in the class B power amplifiers. An RF to dc efficiency of this doubler is 3.4%. The reason for such a relatively low efficiency number compared to amplifiers is that the second harmonic content is much less than the fundamental.

Fig. 4 shows the measured and simulated conversion loss and output power versus frequency. The input power was kept constant at 7 dBm and the bias was adjusted for maximum performance. The peak output power shifted lower by about 4 GHz, but the agreement between measurement and simulation is still good. The output power is better than 2 dBm from 158 to 172 GHz, a 14 GHz, or 8.5% bandwidth.

V. Conclusion

In this letter, a class B MMIC doubler is presented. The doubler uses four-finger AlInAs/GaInAs/InP HEMT devices with 150-μm gate periphery and grounded CPW technology. Design also features a coupled GCPW filter for low frequency oscillation suppression and dc blocking. The total size of this compact chip is 1.32 mm^2. In this first pass design, we have demonstrated

a measured conversion loss of 2 dB at the output power of 5 dBm at 164 GHz. The output power is better than 2 dBm from 158 to 172 GHz, an 8.5% bandwidth. These results are state of the art for HEMT doublers above 100 GHz.

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